~~IDS - 09/26/2003~~

U.S. Department of Commerce, Patent and Trademark Office	Application No.:	
	Filing Date:	
	First Named Inventor:	Soon-Gil Jung
	Group Art Unit:	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Examiner Name:	
(Use several sheets if necessary)	Confirmation No.:	
	Attorney Docket No.:	QKL003 US

U.S. Patent Documents

*Examiner Intials		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
DV	1.	US 6,275,097	Aug. 14, 2001	Liang et al.	327	536	
DV	2.	US 6,509,770	Jan. 21, 2003	Gossmann et al.	327	157	
DV	3.	US 6,535,051	Mar. 18, 2003	Kim	327	536	
DV	4.	US 6,466,070	Oct. 15, 2002	Ross	327	157	
DV	5.	US 6,515,520	Feb. 4, 2003	Kiyose	327	108	

Foreign Patent Documents

		Document	Date	Country	Class	Subclass	Translation	
							Yes	No

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

DV	6.	Ian A. Young, "A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors", IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, Nov. 1992, pp. 1599-1607
DV	7.	Ilya I. Novof, "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±ps Jitter", IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, Nov. 1995, pp. 1259-1266

Examiner: /Don Vo/	Date Considered: 10/25/2006

* Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication with applicant.